(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 December 2003 (11.12.2003)

PCT

(10) International Publication Number
WO 03/103029 A1

(51) International Patent Classification[7]: H01L 21/02

(21) International Application Number: PCT/NL02/00358

(22) International Filing Date: 3 June 2002 (03.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (*for all designated States except US*): **TELEFONAKTIEBOLAGET L.M. ERICSSON** [SE/SE]; Telefonvagen 30, S-126 25 Stockholm (SE).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): **VAN ZEIJL, Paulus, Thomas, Maria** [NL/NL]; Dasstraat 52, NL-7559 AD Hengelo (NL).

(74) Agent: **PRINS, A., W.**; c/o Vereenigde, Nieuwe Parklaan 97, NL-2587 BN The Hague (NL).

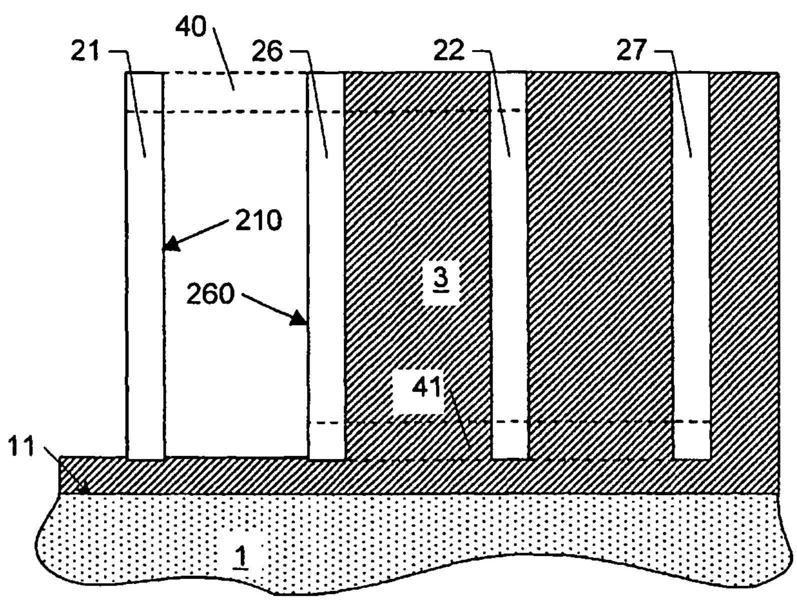
(81) Designated States (*national*): AE, AG, AL, AM, AT (utility model), AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ (utility model), CZ, DE (utility model), DE, DK (utility model), DK, DM, DZ, EC, EE (utility model), EE, ES, FI (utility model), FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK (utility model), SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A CAPACITOR DEVICE FORMED ON A SUBSTRATE, INTEGRATED CIRCUIT COM PRISING SUCH A DEVICE AND METHOD FOR MANUFACTURING A CAPACITOR DEVICE



(57) Abstract: A capacitor device formed on a substrate (1). The capacitor device has at least one first conductor (21-25) with a first capacitor surface (210) and at least one second conductor (26-29) with a second capacitor surface (260). The first and second capacitor surface face each other and are positioned at a distance with respect to each other. The and second capacitor surfaces are electrically isolated from each other. At least one of the capacitor surfaces mainly extend in a direction non-parallel to a substrate surface (11).

WO 03/103029 A1

Title: A capacitor device formed on a substrate, integrated circuit comprising such a device and method for manufacturing a capacitor device.

The invention relates to a capacitor device formed on a substrate and an integrated circuit comprising a capacitor device.

From the United States patent publication 5 939 766 a capacitor device is known. The capacitor is formed on an isolating layer formed over a semiconductor substrate. The capacitor comprises a first layer of metal patterned to form a plurality of first conductors each having two ends and a length there-between. A first connecting electrode is connected to one end of each of the first conductors. Each of the first conductors is electrically isolated from the other first conductors except for the connection formed with the first connecting electrode. The capacitor further has a plurality of second conductors each having two ends and a length there-between and a second connecting electrode connected to one end of each of the second conductors. Each of the second conductors is electrically isolated from the other conductors except for the connection formed with the second connecting electrode. The second conductors are arranged such the plurality of first conductors and the plurality of second conductors are interdigitated. On top of the first layer, an electrically isolating layer is deposited. On top of the electrically isolating layer a second layer of metal is positioned, which is consequently electrically isolated from the first layer. The second layer is similar to the first layer and comprises first and second conductors arranged in an interdigitated manner. The conductors of the second layer are placed such that the first conductors in the first layer face second conductors in the second layer and vice versa.

However, a disadvantage of this known capacitor device is that control and thus reproduction of the capacitor characteristics is difficult. The properties of the known capacitor device are for a significant part determined by the distance between the conductors in a direction perpendicular to the

substrate. This distance is difficult to control. Especially the distance between the first and second layers, and thus the distance between the conductors in the first layer and the conductors in the second layer is difficult to control, because of the topography or 'roughness' of the deposited layers. As is generally known in chip processing, the surface of each layer is not an ideal plane, but has a certain roughness. This roughness increases with the amount of material deposited on the substrate. Hence, the distance between the layers is different to control.

It is therefore a goal of the invention to provide a capacitor device with better controllable characteristics. In order to achieve this goal, the invention provides a capacitor device according to claim 1.

The topography of layers deposited on the substrate has little influence on the characteristics of the capacitor, since the capacitor surface mainly extends in a direction non-parallel to the layers. Thus the thickness of the layers and/or the distance between the layers, does not influence the position of the capacitor surface. Thus, the characteristics are better controllable.

The invention further provides an integrated circuit according to claim 13.

It should be noted that from H. Samavati et al., 'Fractal capacitors', *IEEE journal of solid-state circuits*, vol. 33, no. 12, december 1998, 2035-2041, a linear capacitor using fractal geometries is known. In this paper, a linear capacitor structure has been introduced that uses lateral flux as well as vertical flux to achieve high capacitance per unit area. The structure exploits cross-connected metal layers with a fractal border. The metal layers extend in parallel to the substrate. However, the distance between the metal layers in the direction transverse to the substrate is difficult to control and hence the characteristics of the capacitor structure.

Furthermore, from the United States patent publication 5 208 725, a high capacitance structure in a semiconductor device is known. In the structure described in this '725 publication, two layers of conducting metal

strips are formed upon a semiconductor substrate and an isolating layer. The first layer is formed by two sets of strips. The strips are arranged alternately in parallel to each other. Above and separated from the first layer of conducting strips by an isolating layer, is a second layer of two sets of conducting strips. The conducting strips in the second layer, respectively, overlie the conducting strips of the first layer. This high capacitance structure has the same disadvantage as the capacitor device known from the '766 publication.

Also, from the United States patent publication 5 583 359, a capacitor structure for an integrated circuit is known. This prior art capacitor structure comprises an isolation layer having formed thereon a first electrode defined by a part of a first layer of conductive metallisation; a layer of capacitor dielectric formed thereon provided by part of a first interlayer dielectric; a second electrode defined by part of a second layer of conductive metallisation and overlying the first electrode. In one embodiment, each electrode comprises a main portion defining a plurality of elongate elements, i.e. fingers, each of which are interconnected at one end to form a comb like structure. The fingers are arranged in an interdigitated configuration. This capacitor structure also has the disadvantages of the capacitor device known from the '766 publication.

Specific embodiments of the invention are set forth in the dependent claims. Further details, aspects and embodiments of the invention will be described with reference to the figures in the attached drawing.

Fig. 1 schematically shows a cross-sectional view of an example of a first embodiment of a capacitor device according to the invention.

Fig. 2 schematically shows a cross-sectional view of an example of a second embodiment of a capacitor device according to the invention.

Fig. 3 schematically shows a cross-sectional view of an example of a third embodiment of a capacitor device according to the invention.

Fig. 4 schematically shows a top view of an example of a capacitor device according to the invention with parallel layers.

Fig. 5 schematically shows a top view of an example of a capacitor device according to the invention with pillar shaped conductors.

Figs. 6-8 schematically illustrate by way of a cross-sectional view of an example of a capacitor device according to the invention successive stages of a manufacturing process.

In this application the words 'including' and 'comprising' are used as meaning: 'having but not limited to'.

The example shown in fig. 1 of a first embodiment of a capacitor device according to the invention, comprises first conductors 21,22 and second conductors 26,27. The first and second conductors protrude with respect to the surface 11 of a substrate 1, i.e. the conductors 21,22,26,27 are positioned in a non-parallel direction with respect to said surface. The conductors each have at least one capacitor surface. In fig. 1 the capacitor surfaces of the first conductor 21 and the second conductor 26 are denoted with the numbers 210 and 260 resp. The capacitor surfaces from the first conductors face the capacitor surfaces from the second conductors and vice versa. The first conductors 21,22 are connected to each other via a first connecting electrode 40. The second conductors 26,27 are connected to each other via a second connecting electrode 41.

The first conductors 21,22 are electrically isolated from the second conductors 26,27, in the shown example by an intermediate space 3 between the capacitor surfaces. The intermediate space 3 is filled with a material having a lower electrical conductivity than the material of which the first and second conductors 21,22,26,27 are made, such as for example air or silicon-oxide. The intermediate space may also be empty, that is be a vacuum, as is shown in fig. 1 between the surfaces 210,260 of the conductors 21 and 26. Thus, the conductors 21,22,26,27 constitute the plates of a capacitor. In the shown example, the intermediate space 3 also extends between the first and second conductors and the surface 11 of the substrate 1 and thus electrically isolates the conductors 21,22,26,27 from the substrate 1.

In the example of fig. 1, the first conductors and the second conductors extend in a direction substantially perpendicular to the substrate. Thereby, the distance between the conductors is little dependent on the topology of the layers deposited on the substrate. Hence, the characteristics of the capacitor are little dependent on the topography of the layers deposited on the substrate and are therefore better controllable and reproducible.

Furthermore, because of the alternating arrangement of first conductors and second conductors, the capacitive density is high, since each side of a conductor of one type facing a conductor of the other type acts as a surface of a capacitor plate, so in the shown example each of conductors 22 and 26 acts as two capacitor plates.

Also, a capacitor device according to the invention occupies a small amount of substrate area, especially compared to a capacitor with conductor plates in parallel with the substrate surface. Therefore, a capacitor device according to the invention is cheaper than such a known capacitor, since one of the main factors in the costs of an integrated circuit device is the amount of substrate area occupied.

In fig. 1, the first connecting electrode 40 and the second connecting electrode 41 comprise a strip of electrically conducting material. This may for example be the same material as the material the first conductors and/or the second conductors are made of. Thereby, manufacturing the electrodes does not require extra processing, since the connecting electrodes can be manufactured in the same process as the first conductors and/or second conductors. In use, a voltage difference may be applied between the first conductors 21,22 and the second conductors, 26,27 via the electrodes 40,41.

In the example of fig. 1, each of the connecting electrodes 40,41 connects all the conductors of one type to each other. In use, the voltage difference between the first conductors and the second conductors is therefore substantially the same for all conductors. However, it is likewise possible to

connect the conductors of one type to different voltage sources via separate electrodes.

Often, in chip manufacturing processes, such as for example processes with a deep-submicron resolution, a multiple of interconnect layers is deposited on top of a substrate to obtain electrical interconnections to for example transistor contacts. The interconnect layer comprises parts of a conducting material, such as a metal, which make the desired connection. Such a conducting part in an interconnect layer is also known as an interconnect. The paths of conducting material are separated by a suitable isolating material, such as siliconoxide. In the art, an interconnection formed by a multiple of interconnect layers is known as a multilayer interconnect. Integrated circuits obtained by a manufacturing process in deep-submicron technology with interconnect layers usually contain six or more interconnect layers.

In the example of fig. 2, each of the first conductors 21,22 and second conductors 26-27 extends through a number of interconnect layers 211-214. The interconnect layers 211-214 are separated by interlayer dielectrics 221-223. The conductors are formed by the paths of conducting material in different interconnect layers which are connected to each other at the desired location of the conductor. Thus, the conductors 21,22,26,27 are similar to multi-layer interconnects. Outside the conductors 21,22,26,27 the interconnect layers are of an electrically isolating material, so the different conductors are electrically isolated from each other, except for the electrodes connecting the conductors of one type to each other.

In general, the distance between the interconnect layers is relatively large compared to the distance between the interconnects in one interconnect layer. The conductors formed by connected interconnects thus have a large area and may be positioned close to each other. Thus, a large capacitor surface is obtained on a small chip area when the conductors are formed by connecting interconnect layers and hence a high capacitive density is obtained.

Furthermore, in case the conductors in the capacitor are made from the conducting parts in the interconnect layers the capacitor and the interconnects may be obtained in the same process. Therefore, no extra processing is required in the manufacturing of the capacitor device. Thereby, the costs of the device are reduced.

The conductors may be made from interconnects extending through one, two, three, four, five, six or more interconnect layers. The larger the number of layers, the larger the capacitor area will be, and thus the higher the capacitive density will be. In fig. 3, an example of a capacitor is shown with a varying distance between of the columns, i.e. the surfaces of the first and second conductors are placed at a non-zero angle with respect to each other, as is indicated with dotted lines A. Like the example of fig. 2, the conductors 21-24 are formed from (metal) interconnects extending through interconnect layers 211-214. In practice, the lower metal layers may usually be placed much closer together than the thicker upper metal layers because of the increase of the topography after each processing step. In the art, the topography is the 'roughness' of the surface of the deposited layers. As is generally known in the art, the roughness increases with each deposited layer. The increase in topography effectively results in capacitor plates, e.g. the surfaces of the first conductors and the second conductors, extending under an angle smaller than 90 degrees with respect to the substrate, as is indicated in fig. 3 with dotted lines A.

The first and second conductors in a capacitor device according to the invention may have any shape appropriate for the specific implementation. For example, as is shown in fig. 4, the conductors may be shaped like a plate, that is, have a length and height which are substantially larger than the thickness of the conductors. In fig. 4, the conductors are shaped like straight plates, however they may likewise be curved, wobble shaped or otherwise. Likewise, the conductors may be shaped like pillars, as is illustrated in fig. 5.

In fig. 4 a top-view of an example of a capacitor according to the invention is shown. In fig. 4 first conductors 21-25, and second conductors 26-29 are placed in alternating order. The first conductors are connected to each other via an electrode 40, which lies at one end of the conductors. At the other end, the first conductors are not connected to each other. The second conductors are connected to each other via a second connecting electrode 41, which is connected to the second conductors at an end of the second conductors remote from the first connecting electrode. Thus, seen from the top view, the capacitor device comprises two comb-like structures of which the teeth are placed between each other, i.e. the conductors are interdigitated.

In the example of fig. 4, the first conductors 21-25 and the second conductors 26-29 are positioned substantially parallel to each other. The first conductors may also be placed in a non-parallel direction with respect to the second conductors. Also, some of the first conductors, or some of the second conductors, may be non-parallel with respect to the other first conductors or second conductors.

Fig. 5 shows a top-view of an example of a capacitor device according to the invention with pillar shaped conductors. In the example of fig.5, the first conductors 21-25 and the second conductors 26-29 are placed in an alternating manner, like a checkerboard. The first conductors 21-25 are connected to each other via the first electrode 40. The second conductors 26-29 are connected to each other via a second electrode 41. In the example, the second electrode 41 is electrically isolated from the first electrode 40 and lies on top. The electrodes 40,41 each extend in a single interconnect layer. Because of the checkerboard-like positions of the pillar-shaped conductors 21-29, the capacitance of the capacitor is high, since each conductor of one type faces more conductors of the other type. For example the first conductor 23 is surrounded by four second conductors 26-29. Hence the capacitor area and capacity of the capacitor device of fig. 5 is high.

The capacitance of a capacitor device according to the invention may be calculated from the equation.

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

where C is the total capacitance, $_0$ and $_r$ are the dielectric constants, A is the total area of the capacitor and d is the distance between the plates of the capacitor. The total area A of the capacitor is defined as length*height*number of conductors. For example, using dielectric constants $_0$=8.9e-12, $_r$=4, a surface area A of 13×10μm×4.1μm (this is equal to 13 stripes of 10μm length and 4.1um height, only the first four metal interconnect layers being used) and d=0.4μm, gives a capacitance of 47.4 fF (femto Farad) or 0.47 fF/μm^2.

Layout-extraction for such a layout may further increase the value to 47.76 fF. Layout-extraction is a method wherein after drawing a layout of a device, the total capacitance between any node in the layout is calculated. The parasitic capacitances (from capacitor-nodes to ground) are below 7% of the nominal capacitance value. Current processes have parasitic capacitances ranging from 5% to 20%. Using six instead of four interconnect layers gives an extracted capacitance of 0.63 fF/um^2. The capacitance density in a process with an increased resolution, such as for example a 0.13μm MOS process , results in an even higher capacitance density. Using $_r$=3.6, A=13×10μm ×2.35μm (13 stripes of 10μm length and 2.35μm height, four interconnect layers used) and d=0.2μm gives a capacitance of 48.9 fF or 0.489 fF/μm^2.

A capacitor device according to the invention may be manufactured in various ways. An example is illustrated in figures 6-8. First, a first isolating layer 31 is deposited on a substrate 1. On top of the first isolating layer 31 a first interconnect layer is deposited. After the deposition of the first metal interconnect layer, a number of separated pillars 231-234 is formed, for example by etching the first metal interconnect layer or removing unexposed photo-resist by means of an appropriate solvent. Thereafter a second isolating

layer 32 is deposited. Fig. 6 shows an example of a capacitor device before the deposition of the second isolating layer 32.

Fig. 7 shows the capacitor device after deposition of the second isolating layer. After deposition, the isolating layer 32 partially removed, for example by locally etching the material, to obtain open spacings from the surface of the isolating layer 32 to the pillars 231-234 which are to form the conductors of the capacitor device.

Thereafter, a second metal interconnect layer is deposited on top of the third isolating layer 33. The second metal interconnect layer fills the spacing on top of the separated pillars. The capacitor device then looks as depicted in fig. 8. This process may be repeated until the desired size of the capacitor is obtained. During this process, also electrodes connecting the first conductors or the second conductors to a voltage source are provided. After addition of a layer, the device may be planarised using chemical mechanical polishing.

It should be noted that after reading the above, several modifications should be apparent to the person skilled in the arts. Especially, it should be apparent that the conductors may be oriented in a non-parallel way with respect to each other. Also, a capacitor according to the invention may comprise one or more conductors with surfaces substantially parallel to the substrate surface. Furthermore, it should be apparent that each layer may be made of different materials, for example if the first metal interconnect layer is of copper and the second interconnect layer of aluminium, the first conductor and/or the second conductor may be made out of both materials. Also, it should be apparent that the conductors may be made of any conducting material, such as a conducting plastic, a carbon-base conductor or a superconducting material, such as NbTiN. Also, the conductors may be made of a semiconductor material such as Si, optionally doped with some dopant such as boron. Likewise, the intermediate space may be empty or filled with any suitable material, such as undoped Si, Silicon Oxide, Air or otherwise. Furthermore, the conductors and the intermediate space may have any suitable shape, such

as curved, trapezoid or otherwise . Also, a capacitor device according to the invention may be manufactured in any type of process, such as CMOS, BiCMOS, SiGe, GaAs or otherwise.

Claims

1. A capacitor device formed on a substrate (1), comprising: at least one first conductor (21-25) with a first capacitor surface (210); at least one second conductor (26-29) with a second capacitor surface (260), which first and second capacitor surface face each other and are positioned at a distance with respect to each other and which first and second capacitor surfaces are electrically isolated from each other, and wherein at least one of the capacitor surfaces mainly extend in a direction non-parallel to a substrate surface (11).

2. A capacitor device as claimed in claim 1, wherein at least one of said first and second conductor surfaces (210,260) extends in a substantially perpendicular direction with respect to said substrate surface (11).

3. A capacitor device as claimed in claim 1 or 2, wherein said at least one first conductor (21-25) and said at least one second conductor (26-29) contain a metal.

4. A capacitor device as claimed in any one of the preceding claims, wherein an intermediate space (3) between the first and second capacitor surface is filled with a material containing silicon-oxide.

5. A capacitor device as claimed in claim 1 or 2, wherein said at least one first conductor (21-25), said at least one second conductor (26-29) and an intermediate space (3) between the first and second capacitor surface contain silicon.

6. A capacitor device as claimed in claim 5, wherein

the silicon in said at least one first conductor (21-25) and said at least one second conductor (26-29) differs from the silicon of said intermediate space (3) by a doping of the silicon.

7. A capacitor device as claimed in any one of the preceding claims, wherein
said at least one first conductor (21-25) and said at least one second conductor (26-29) extend through at least two interconnect layers (211-214) of a chip.

8. A capacitor device as claimed in any one of the preceding claims, including a multiple of first conductors (21-25) and second conductors (26-29).

9. A capacitor device as claimed in claim 8, at least including:
at least a first comb-like structure (40, 21-25) comprising said first conductors (21-25) connected at one side to each other via a first connecting electrode (40),
at least one second comb-like structure (41, 26-29) comprising said second conductors (26-29) connected at one side to each other via a second connecting electrode (41), and
in which capacitor at least one of said second conductors extends at least partially between at least two of said first conductors.

10. A capacitor device as claimed in any one of the preceding claims, wherein said first and second conductor surface (210,260) are substantially parallel to each other.

11. A capacitor device as claimed in any one of the claims 1-9, wherein said first and second capacitor surface (210,260) are positioned in non-parallel with respect to each other

12. A capacitor device as claimed in any one of the preceding claims, wherein at least one of the at least one first conductor and the at least one second conductor has a tapered shape.

13. An integrated circuit comprising a number of electrical components, said electrical components including at least one capacitor device as claimed in any one of the preceding claims.

14. A method for manufacturing a capacitor device in an integrated circuit on a substrate comprising:
depositing on the substrate at least one layer of conducting material
depositing on the substrate at least one layer of isolating material,
whereby at least one first conductor (21-25) with a first capacitor surface (210); at least one second conductor (26-29) with a second capacitor surface (260) are formed, which first and second capacitor surface face each other, and whereby an intermediate space (3) is formed between the first and second capacitor surface which separates said first conductor and said second conductor, said intermediate space having a lower electrical conductivity than said first conductor and said second conductor,
and whereby
at least one of the capacitor surfaces mainly extends in a direction non-parallel to a substrate surface (11).

15. A method as claimed in claim 14, wherein at least one of said at least one layers of conducting material is also used to form interconnects in the integrated circuit.

Fig. 1

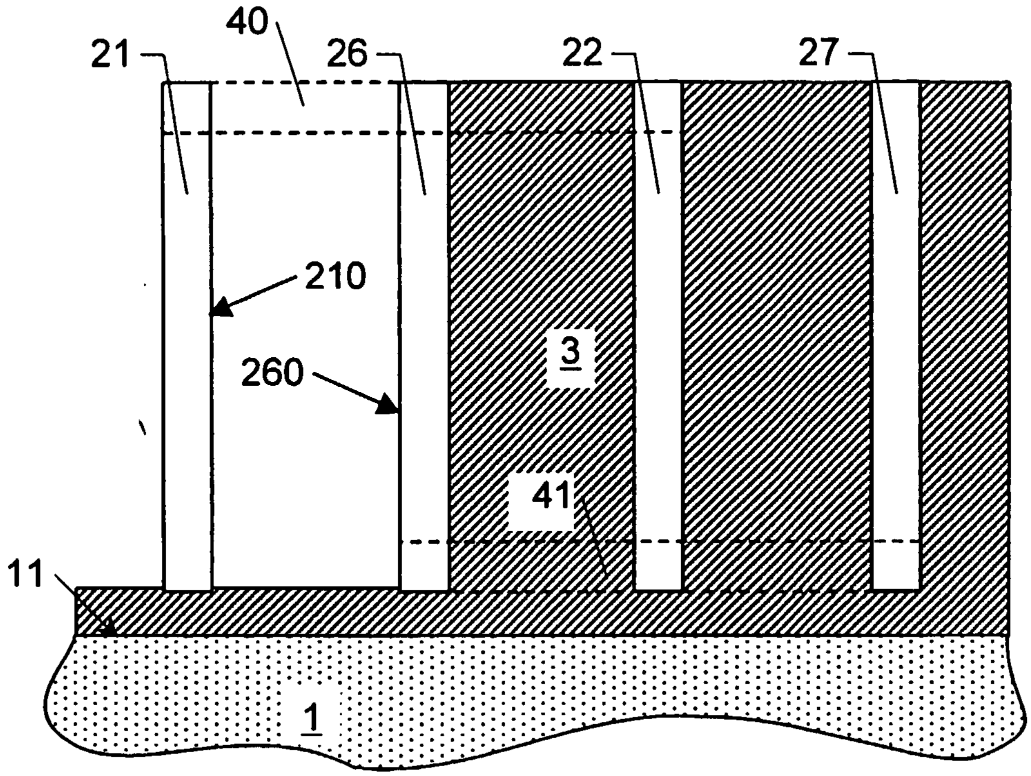

40
21
26
22
27
210
3
260
41
11
1

Fig. 2

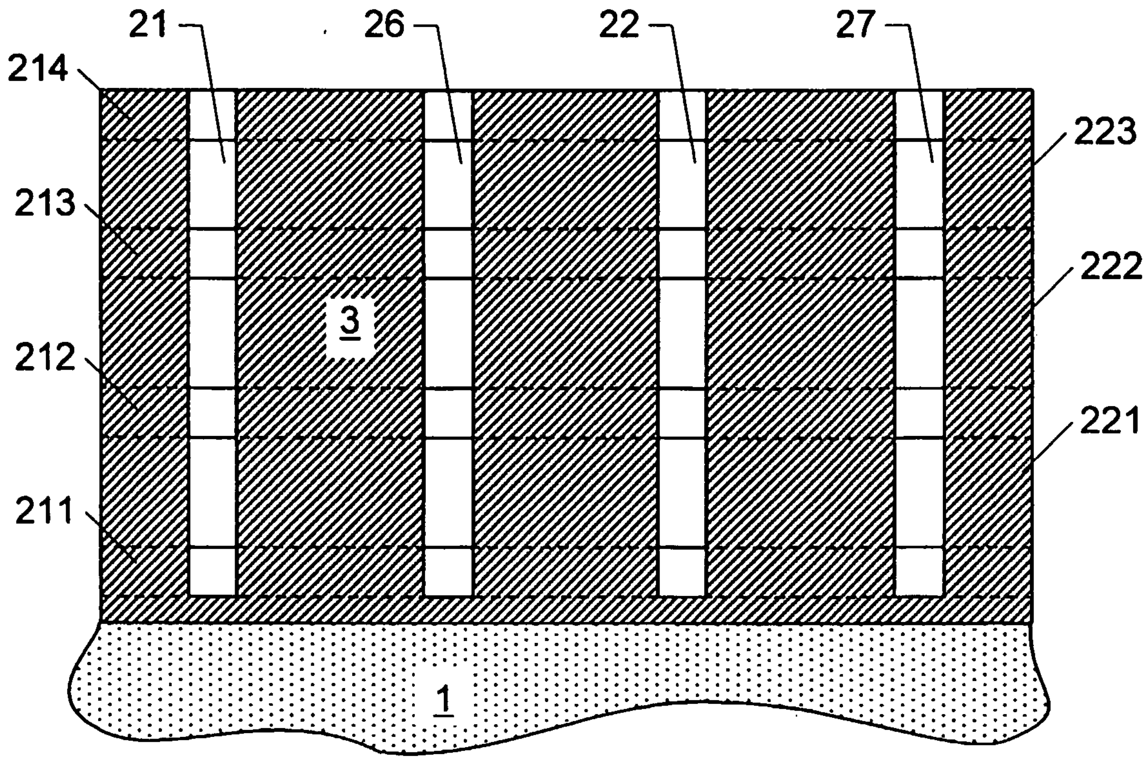

21
26
22
27
214
223
213
222
3
212
221
211
1

Fig. 3

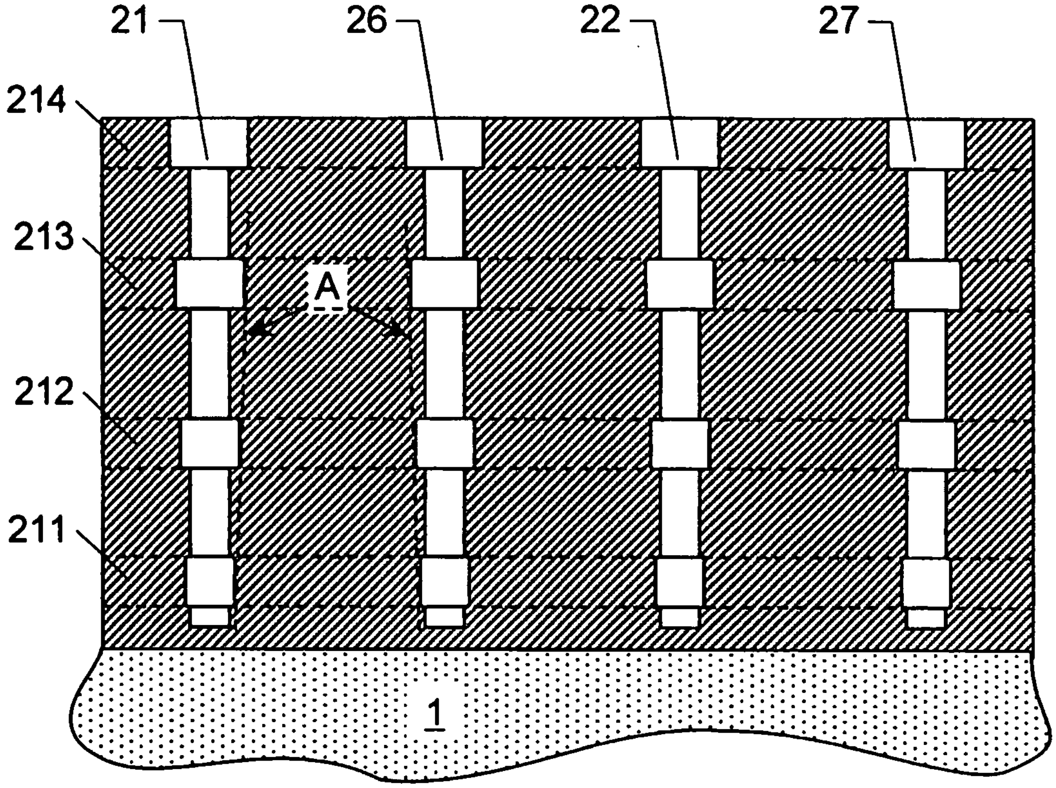


Fig. 4

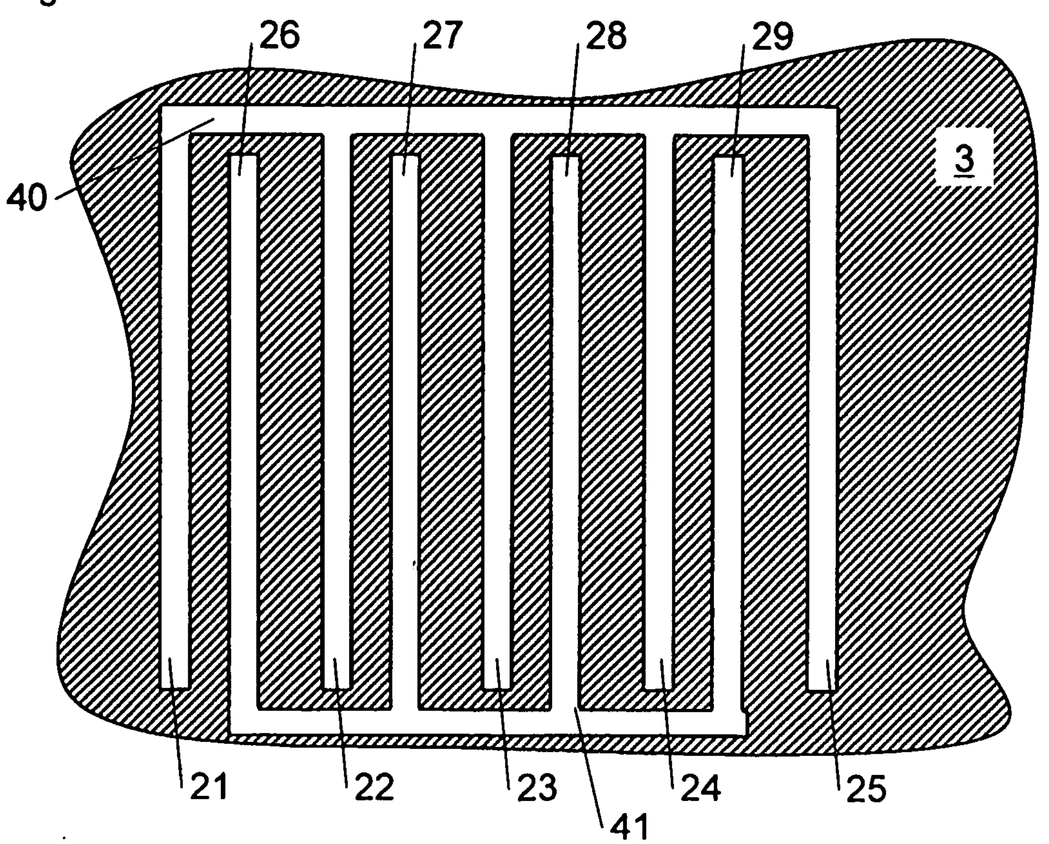


Fig. 5

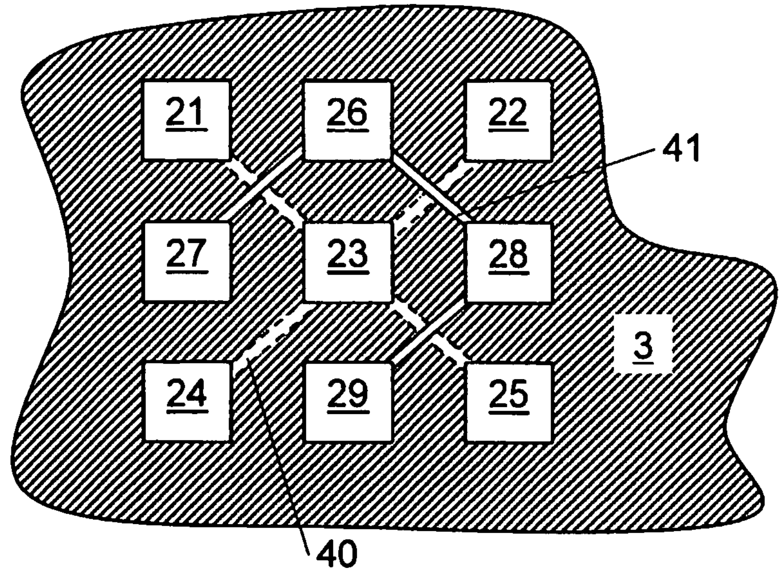


Fig. 6

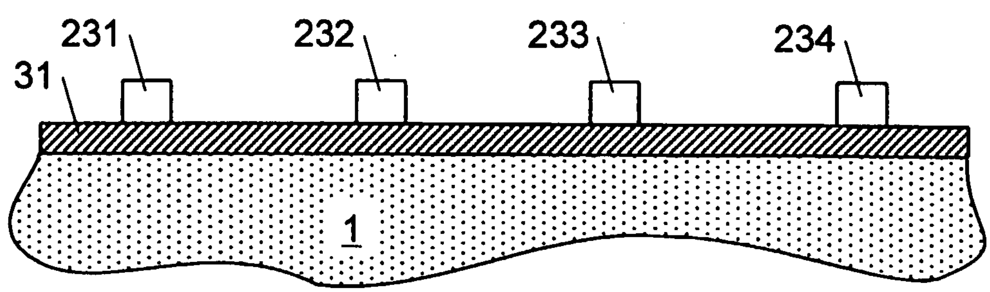


Fig. 7

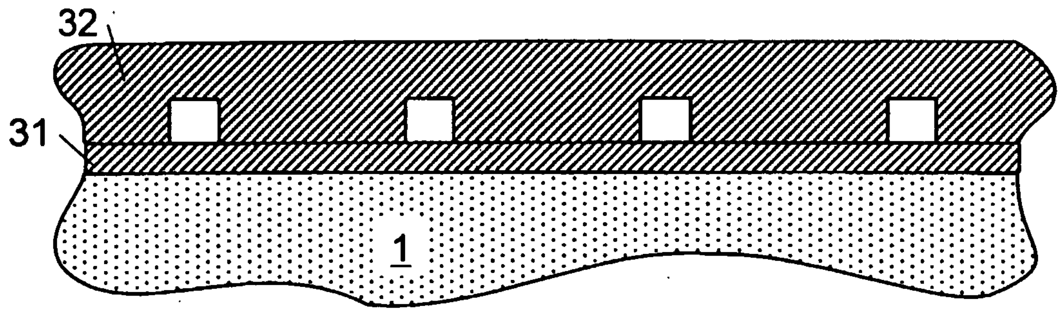
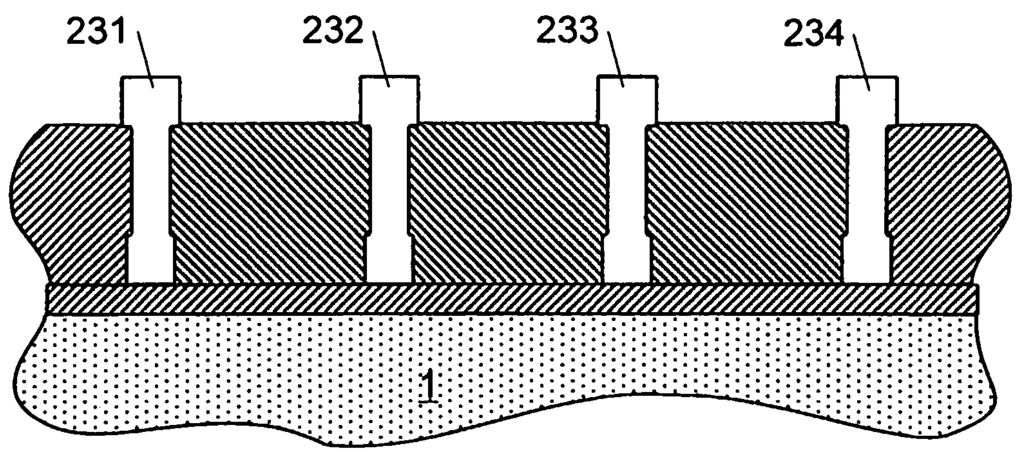


Fig. 8



INTERNATIONAL SEARCH REPORT

PCT/NL 02/00358

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02 27770 A (CALIFORNIA INST OF TECHN) 4 April 2002 (2002-04-04) figures 2,3	1-3,7-12
X	WO 01 99163 A (KONINKL PHILIPS ELECTRONICS NV) 27 December 2001 (2001-12-27) abstract; figure 2	1-3, 8-10,13
X	WO 01 75983 A (KONINKL PHILIPS ELECTRONICS NV) 11 October 2001 (2001-10-11) figures 3,4	1-3,13

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2003	19/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Königstein, C

INTERNATIONAL SEARCH REPORT

PCT/NL 02/00358

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MATSUO N ET AL: "SPREADED-VERTICAL-CAPACITOR CELL (SVC) FOR BEYOND 64MBIT DRAMS" PROCEEDINGS OF THE INTERNATIONAL ELECTRON DEVICES MEETING. WASHINGTON, DEC. 8 - 11, 1991, NEW YORK, IEEE, US, 8 December 1991 (1991-12-08), pages 91-473-476, XP000342181 ISBN: 0-7803-0243-5 the whole document ---	1,13
A	DE 100 41 620 A (MITSUBISHI ELECTRIC CORP) 28 June 2001 (2001-06-28) the whole document -----	14,15

INTERNATIONAL SEARCH REPORT

PCT/NL 02/00358

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 0227770	A	04-04-2002	US	2002093780 A1	18-07-2002
			AU	8908001 A	08-04-2002
			WO	0227770 A2	04-04-2002
WO 0199163	A	27-12-2001	WO	0199163 A2	27-12-2001
			EP	1228527 A2	07-08-2002
WO 0175983	A	11-10-2001	US	6297524 B1	02-10-2001
			WO	0175983 A2	11-10-2001
DE 10041620	A	28-06-2001	JP	2001177070 A	29-06-2001
			DE	10041620 A1	28-06-2001
			TW	478141 B	01-03-2002